AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended): A method comprising:

determining an optimum splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in ~~a~~ the set of equations representing the PLA;

dividing a set of equations representing a PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA;

applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and

controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA.

Claim 2 (Original): The method of claim 1, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 3 (Original): The method of claim 1, further comprising merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA.

Claims 4-5 (Canceled)

Claim 6 (Original): The method of claim 1, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 7 (Original): The method of claim 1, further comprising delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA.

Claim 8 (Canceled)

Claim 9 (Original): The method of claim 1, wherein determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design.

Claim 10 (Currently Amended): A method comprising:

determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting

variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

dividing the set of equations representing the PLA into equations representing the at least two sub-PLAs;

merging outputs of the equations representing the at least two sub-PLAs;

determining a topological circuit representation of the equations representing the at least two sub-PLAs;

applying gating logic to the topological circuit representation of the at least two sub-PLAs; and

controlling power consumption in the topological representation of the at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption,

wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

Claim 11 (Original): The method of claim 10, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 12 (Original): The method of claim 10, wherein the equations representing the plurality of sub-PLAs are divided recursively based on a determined optimum splitting variable for each equation representing a sub-PLA.

Claim 13 (Original): The method of claim 12, wherein each product of the equations representing the plurality of sub-PLAs is obtained by omitting literals in the equations representing the PLA.

Claim 14 (Original): The method of claim 13, wherein a product of the omitted literals is used in the topological circuit representation of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs.

Claim 15 (Canceled)

Claim 16 (Original): The method of claim 12, wherein the step of determining the optimum splitting variable for each of the equations representing the sub-PLA further comprises avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA.

Claim 17 (Currently Amended): A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, said first sub-PLA and said second sub-PLA each have an AND plane and an OR plane, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in ~~a~~ the set of equations representing the PLA;

divide the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determine a topological circuit representation of first sub-PLA and the second sub-PLA;

apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and

control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein the topological circuit representation an OR plane of the first sub-PLA is interleaved with an OR plane of the second sub-PLA.

Claim 18 (Original): The program storage device of claim 17, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 19 (Original): The program storage device of claim 17, further comprising instructions that cause the machine to merge an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein the instruction that causes the machine to merge the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA, forms a logical equivalent of the equations representing the PLA.

Claims 20-21 (Cancelled)

Claim 22 (Original): The program storage device of claim 17, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 23 (Canceled)

Claim 24 (Currently Amended): A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

divide the set of equations representing the PLA into equations representing the at least two sub-PLAs;

merge outputs of the equations representing the at least two sub-PLAs;

determine a topological circuit representation of the equations representing the at least two sub-PLAs;

apply gating logic to the topological circuit representation of the at least two sub-PLAs; and

control power consumption in the topological circuit representation of the at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption,

wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

Claim 25 (Original): The program storage device of claim 24, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 26 (Original): The program storage device of claim 24, wherein the instruction causing the machine to divide the equations representing the plurality of sub-PLAs divides recursively based on a determined optimum splitting variable for each equation representing a sub-PLA.

Claim 27 (Original): The program storage device of claim 24, wherein the instruction causing the machine to determine the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the equations representing the PLA; and

selecting a column with smallest overhead in the AND plane of the equations representing the PLA.

Claim 28 (Canceled)

Claim 29 (Currently Amended): A method comprising:

determining an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

dividing the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA;

applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA.

Claim 30 (Previously Presented): The method of claim 29, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 31 (Previously Presented): The method of claim 29, further comprising merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the

equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA.

Claim 32 (Previously Presented): The method of claim 29, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 33 (Previously Presented): The method of claim 29, further comprising delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA.

Claim 34 (Canceled)

Claim 35 (Previously Presented): The method of claim 29, wherein determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design.

Claim 36 (Currently Amended): A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

divide a set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determine a topological circuit representation of the first sub-PLA and the second sub-PLA;

apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and

control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein in the topological circuit representation an OR plane of the first sub-PLA is separated from an OR plane of the second sub-PLA.

Claim 37 (Previously Presented): The program storage device of claim 36, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 38 (Previously Presented): The program storage device of claim 36, further comprising instructions that cause the machine to merge an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA,

wherein the instruction that causes the machine to merge the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA, forms a logical equivalent of the equations representing the PLA.

39. (Previously Presented) The program storage device of claim 36, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 40 (Canceled)